UCRL- 94494
PREPRINT

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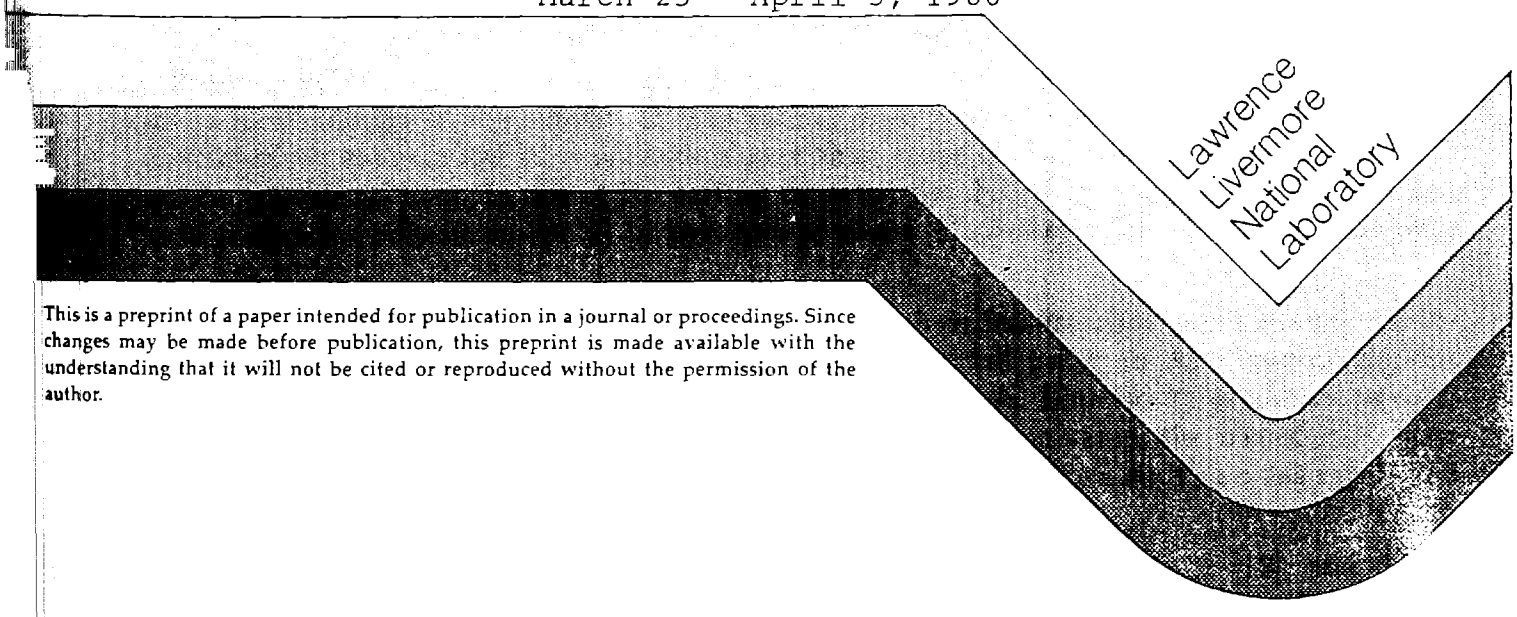
This paper was prepared for submittal to:
The Les Houche Winter School, Les Houche, France

March 25 - April 5, 1986



Fabrication of Gate Array Interconnect Structures Using Direct-Write Deposition Processes

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Abstract

General principles of laser direct-write deposition processes are reviewed. Device interconnection of CMOS gate arrays by means of computer-controlled, laser-induced thermochemical surface reactions is described. Maskless, automated, five-minute interconnection of 1000 gate CMOS array dies is described using discretionary laser-induced chemical vapor deposition. Eight 125-stage ring oscillators written on a single CMOS gate array die were shown to have the device-limited performance of similar patterns manufactured by a photolithographically patterned aluminum-silicon alloy. These results suggest the feasibility of using this method, Laser Pantography (LP), for rapid implementation of prototype and limited volume semi-custom VLSI circuits immediately after their design is completed.

I. Introduction

The desirability of using local, laser microchemical techniques for maskless fabrication and alteration of integrated circuits has been recognized. Laser direct-write processes capable of local deposition or etching of a wide variety of materials on semiconductor substrates have been demonstrated [1-7]. They use a focused laser beam to supply energy to a micron-scale reaction zone. The local reaction of the ambient gas may be driven by direct photo-absorption, or by local heating of the substrate. The former class of reactions (photolytic), which have characteristic rates orders of magnitude slower than those of the latter class (pyrolytic), will not be considered here. In one of the earliest reported pyrolytic experiments, a CO_2 laser was used to deposit polysilicon (poly) by pyrolysis of silane [8]. However, the deposited lines were ~50 μm wide.

The use of shorter wavelength lasers is needed to achieve feature sizes small enough for integrated circuits (ICs). In 1981, two groups [9,10] reported using an Ar^+ laser to deposit micron-scale poly lines (from silane) at speeds up to 100 μm/s. Linewidths as narrow as ~0.2 μm have been achieved [11]. In consideration of these reaction rates, the use of local laser microchemical deposition was suggested mainly for minor alterations, such as mask repair and restructuring of previously lithographed ICs.

To date, single-trace circuit alteration [12], photolithography mask repair [13], and device connection [14] on CMOS gate arrays have been demonstrated, as well as the fabrication of single devices by laser deposition, doping, and etching [15]. Our work has emphasized rapid reactions capable of writing rates of at least 1000 μm/s laterally, and which are suitable for fabrication of IC interconnects. We previously reported a poly deposition reaction in this line-writing speed range [14]. This paper reports the use of that reaction to rapidly interconnect complex circuits on 1000 gate CMOS arrays.

This work was performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. W-7405-

II. Chemical Reactions for Laser Deposition

A variety of laser-induced interconnection formation processes has been studied [1-10]. These fall into two broad classes: photolytic and pyrolytic processes. The photolytic processes are based on local laser-induced photodecomposition reactions occurring either at the substrate and/or in the gas phase. The pyrolytic processes are based on chemical vapor deposition reactions which occur due to local heating from a focused laser beam incident on the substrate. In applications for IC manufacturing, pyrolytic processes have the advantages of exhibiting substantially higher rates with presently available laser technology and, since they are based on chemical reactions already used in IC manufacturing, they interface more readily with typical IC processes and materials.

There are two basic groups of laser-driven pyrolytic processes which might be applied to interconnection of device structures in integrated circuits. One group is the surface-catalyzed unimolecular thermodecomposition reactions, such as those involving carbonyls and silanes. Examples of particular interest are

$$Ni(CO)_4 \rightarrow Ni(s) + 4CO \tag{1}$$

$$SiH_4 \rightarrow Si(s) + 2H_2 \tag{2}$$

$$Si_2H_6 \rightarrow 2Si(s) + 3H_2 \tag{3}$$

These reactions are based on reactants which at room temperature have vapor pressures of at least a few hundred Torr and deposit materials which have high melting points, thus potentially allowing relatively fast deposition rates (as explained below). The other groups of reactions are "bimolecular" reactions, typically involving reduction of metal halides. Two reactions of this type are

$$WF_6 + 3H_2 \rightarrow W(s) + 6HF \tag{4}$$

$$WF_6 + \frac{3}{2}Si(s) \rightarrow W(s) + \frac{3}{2}SiF_4 \tag{5}$$

Since tungsten and tungsten silicide are attractive interconnect materials for next-generation VLSI/ULSI circuitry, processes which rapidly generate high quality W and WSi_2 interconnections could be very useful.

Tungsten deposition by silicon reduction of tungsten hexafluoride [reaction (5)] offers the interesting possibility of being used as a bulk process following direct-write of a silicon interconnect structure by a laser process based on reactions (2) and (3). This approach could greatly increase the conductivity of the laser-patterned polysilicon structure at the cost of only a small amount of processing.

An inherent advantage of direct-write laser processes is their sequential nature which allows on-line changes of the interconnect structures for circumventing defects in devices or interconnect structures. In general, such changes can require both etching and deposition processes. For removal of silicon and various metal structures, processes based on halogen containing gases have been studied and reported [20,21,22].

Reaction Kinetics for Laser Deposition

Since laser-induced deposition processes proceed in a sequential manner, one of the most important issues to be considered is reaction kinetics. Laser-induced pyrolytic deposition processes can be thought of as involving six consecutive steps:

1. Local heating of the substrate by absorption of laser energy.
2. Transport of the reactant gas to the laser-heated portion of the substrate;
3. Adsorption of the reactant on the substrate surface;
4. Decomposition of the reactant gas on the heated portion of the surface;
5. Desorption of the volatile product from the heat surface; and
6. Transport of the product gas away from the substrate surface.

The rate-limiting factors of such processes are often set by the chemical reaction rate after the nucleation phase of the process which is described by an Arrhenious-type relation of the form:

$$R = R_o e^{-T_A/T} P^n \tag{6}$$

where P is the reactant gas pressure, T is the substrate temperature, n is the reaction order and T_A is the activation temperature.

At low temperatures, the deposition rates are limited by the surface reaction rate of (6). Clearly this process can be accelerated by increasing the incident laser power, and hence the surface temperature. As this is done, the surface reaction rate may eventually outstrip the ability of the gas to deliver reactants and/or to remove reaction products. As a result the deposition rate does not continue to climb with laser power, but eventually saturates.

A general treatment of the transport of reactant and product gases during laser deposition is difficult. The character of the transport depends critically on two parameters: whether the reaction absorbs or liberates gas molecules; and the ratio of the hot spot size, ρ, to the molecular mean-free path, λ.

If the Knudsen number, $Kn = \lambda/\rho$, is very large, then the effects of gas transport are easily calculated. In this molecular flow regime, reactant species are supplied to the surface at a rate of

$$F_i = \frac{1}{4} n_i v_i \tag{7}$$

where F_i is the number of molecules per second per area striking the surface, v_i is the average molecular speed of reactant species i, and n_i is its molecular density.

In this flow regime, the ejected molecules free-stream away from the hot spot, creating a local atmosphere of reaction products. However, because the ejection speeds are greater than those of reactant gases and are more effectively directed, these product densities are low, and should not choke the reaction. Hence, in the molecular flow regime, the deposition rate saturates at a level dictated by the slowest influx rate. For Si deposition by silane, this rate is $\approx$75 μm sec^{-1} Torr^{-1}.

While the molecular flow regime is easy to analyze, it can only be assumed for large Knudsen numbers, which for micron-scale spots implies pressures below about 10 Torr. Since we generally operate at higher gas densities in order to increase the deposition rate, the actual molecular flow is strongly influenced by gas collisions.

Accurate calculation of the gas transport in the fluid regime is difficult, involving both diffusion and convection of multiple species. The analysis is even more complicated in the $p \approx 100$ Torr regime, in which transport is in transition between the molecular and fluid regimes. Accordingly, we will only qualitatively discuss transport at such gas densities.

The flow will strongly depend upon the reaction balance of gas molecules. If the reaction absorbs more gas molecules than are liberated, then reactants can be supplied to the hot spot at sonic velocities. The specific influx rate ranges from the molecular limit of (7), to a rate about 70% higher in the fluid limit. If there are no product gases, the gas transport rate can then be monotonically increased by raising the gas density, until the surface rate of (5) is reached. Product gases will have to diffuse away from the hot spot against the reactant influx, and if present can thus choke off the reaction.

Most reactions, including the ones discussed earlier, liberate at least as many molecules as they absorb. In the case where there is no net molecular generation, the gas convection is relatively weak. Here the transport of reactants and products is a diffusion limited process. This case was analyzed for constant gas diffusion constants in [3]. The specific transport rates scale as D/ρ, a considerably lower velocity than the sonic rate. Furthermore, one cannot arbitrarily increase the deposition rate by increasing gas density. Once the reactant density dominates the total density, then the diffusion coefficient will decrease, and the transport limited deposition rate will saturate.

IV. Gate Array Interconnect Process Description and Apparatus

The gate array, made by the *selective oxide silicon gate CMOS process*[16], is designed for single level metallization with underlying poly tunnels for routing.

A ~1 μm thick aluminum-silicon alloy on the gate array wafer is pre-patterned using conventional photolithography to leave I/O pads with interconnected drivers, power distribution, plugs in the contact vias, and a few simple logic gates interconnected at the periphery. After the metal patterning is complete, the surface is coated with a thin film of undoped amorphous silicon (a-Si). For this particular gate array personalization technology no loss of generality is suffered by prepatterning the metal as described in the preceding paragraph because this portion of the metallization is independent of the circuit design. The few interconnected gates are added as a process control monitor to allow electrical pretesting of each die before the laser direct-write personalization step.

The substrates are personalized by discretionary laser-induced pyrolytic deposition of degenerately doped poly. The reactant gas used in this process is a mixture of silane, disilane, and a dopant gas. Phosphine is used when n-type doping is desired. Diborane is substituted for phosphine to obtain p-type doped poly. Total reactant gas pressure of ~1 atmosphere is typically used. The deposited material has a resistivity of $\sim 3 \times 10^{-3}$ ohm-cm, as reported previously [14]. The poly line segments, deposited at a lateral scan rate of 1000 μm/s in all cases, are generally ~3-4 μm wide and ~1 μm high (Fig. 1).

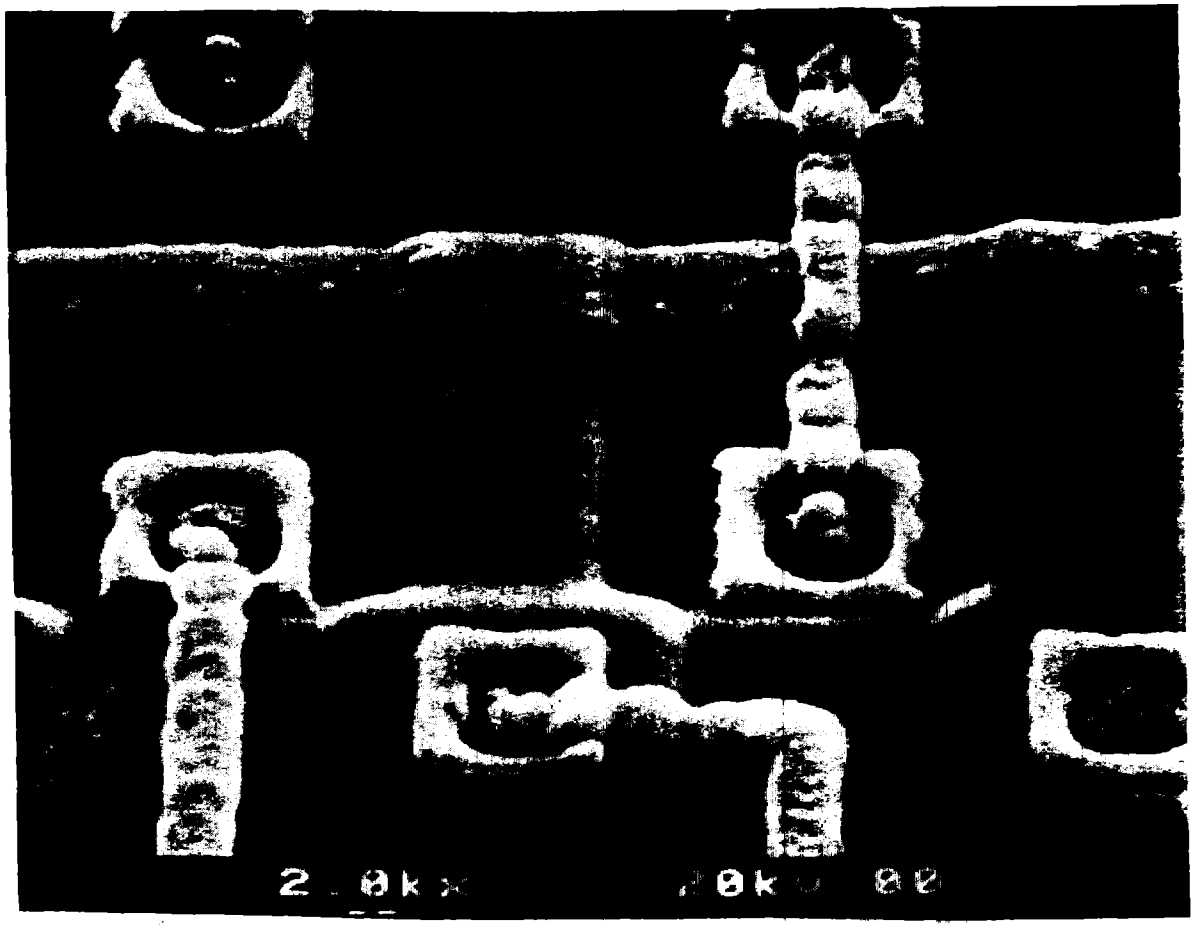

Figure 1. SEM of laser deposited polysilicon interconnects on a CMOS gate array. Photolithographic preprocessing of Al-Si alloy includes power bus (large horizontal trace) and filled vias.

The apparatus used for laser-writing in the work being reported here is similar to that previously described 17, with a 5145Å Ar^+ laser focused through the reaction chamber window by a 20X microscope objective to a ~1 μm spot on the substrate. One new feature is to move the beam over a 512 micron square field by an orthogonal pair of acousto-optic scan crystals. Direct writing is accomplished in real time using programmable hardware which controls beam position, writing speed, and beam power.

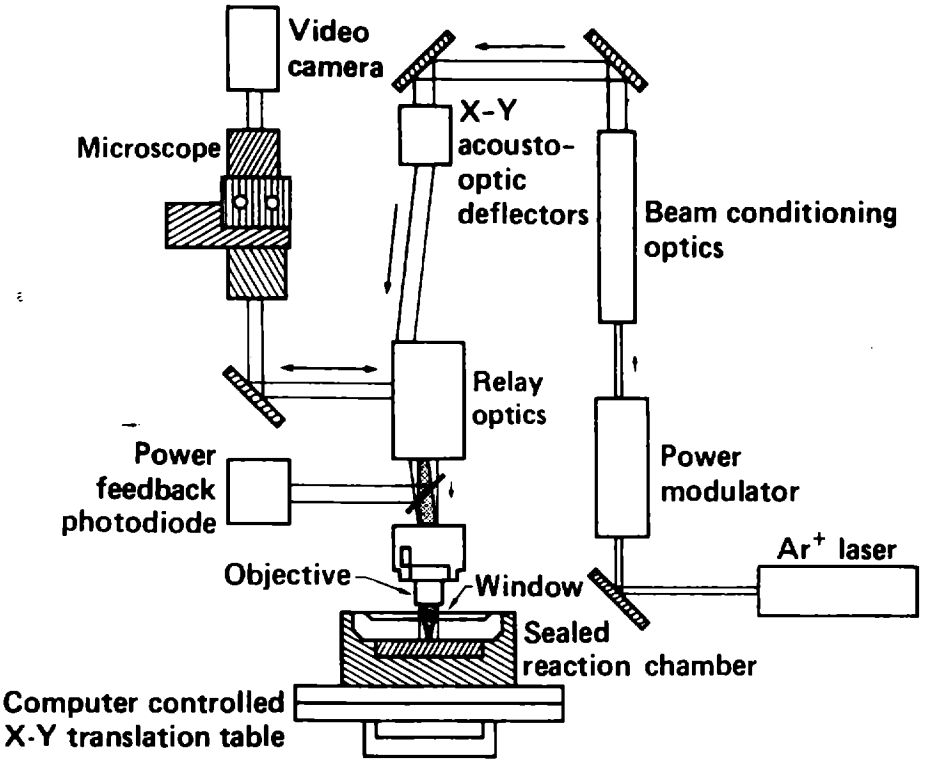

Figure 2. Layout of apparatus used for polysilicon direct write by solid state laser scanning. (The darker stipling indicates the path of the laser beam. The lesser shaded path is that of white light for imaging.)

The software required to automatically generate the command sequences necessary for discretionary laser writing of complex patterns has been developed. There are two principal software packages which do this: they are known as the Assembler and the Monitor.

The Assembler translates an industry-standard CIF (Caltech Intermediate Format) file, which contains a geometric description of a circuit design, into a set of instructions called scan code. This scan code specifies the position, velocity, direction, and power level of the laser beam. The Assembler is cognizant of the special processing required for certain device features and alters the scan code process parameters to account for this. The scan code also includes the information to position and align the substrate after each 512 micron square scan field has been written.

The Monitor is a real-time computer control system which positions the substrate, controls the direct-write process, and provides a user interface to the apparatus. It accepts scan code produced by the Assembler and uses it to drive the scanner, beam power controller, and X-Y translation slides. The slides reposition the reaction chamber for each scan window. One or more gate arrays may be patterned automatically using the Monitor under high-level operator control.

Once a circuit is designed and physical placement and routing are complete, a minicomputer running the software described above generates the scan code necessary to run the LP apparatus in less than one hour.

V. RESULTS

Digital logic circuitry patterned in aluminum-silicon alloy fabricated by photolithography was tested and compared with similar circuitry patterned by the laser direct-write process described above.

Ring oscillators consisting of 17, 35, and 125 stages were fabricated. The periods were found to have the expected 1:2:7 ratios. The nominal cycle time obtained by dividing the periods by the number of stages was ~6 ns in all cases (Fig. 3), suggesting gate delay times including signal propagation to the next gate of about half that time. A light micrograph of a typical 17 stage ring oscillator segment fabricated by the LP process is shown in Fig. 4. Laser induced damage, poor for circuits fabricated with laser writing processes were searched for by comparing identical ring-oscillator circuits fabricated by conventionally-lithographed aluminum-silicon. No significant difference in oscillation frequency between laser- and conventionally-interconnected gate-arrays was observed. Furthermore, both n-type and p-type laser-deposited poly ring-oscillators had the same oscillation frequency.

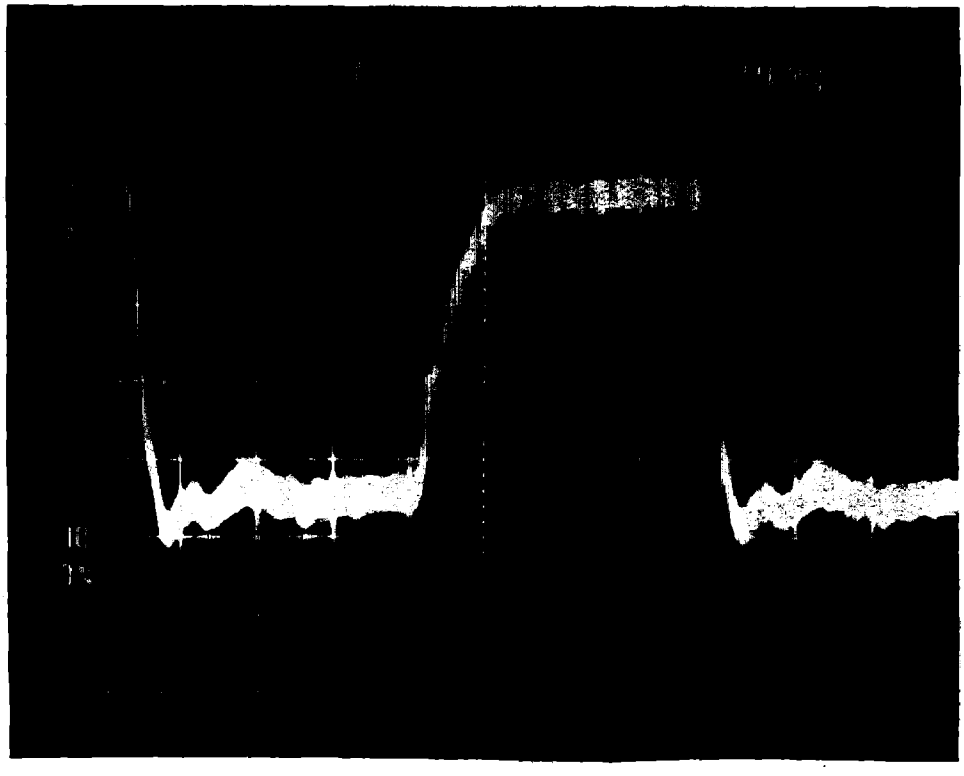

Figure 3. Oscillograph of output of 125-stage ring oscillator interconnected by the laser direct-write process, operating at 5 volts. The period of 750 ns reveals an average inverter cycle time of 6 ns.

On one die consisting of eight 125-stage ring oscillators, an open circuit was observed during electrical testing. This gap was closed by a spot of laser-deposited poly to yield a properly functioning circuit. The postulated repair capability of laser direct-write processes [3] was thus verified.

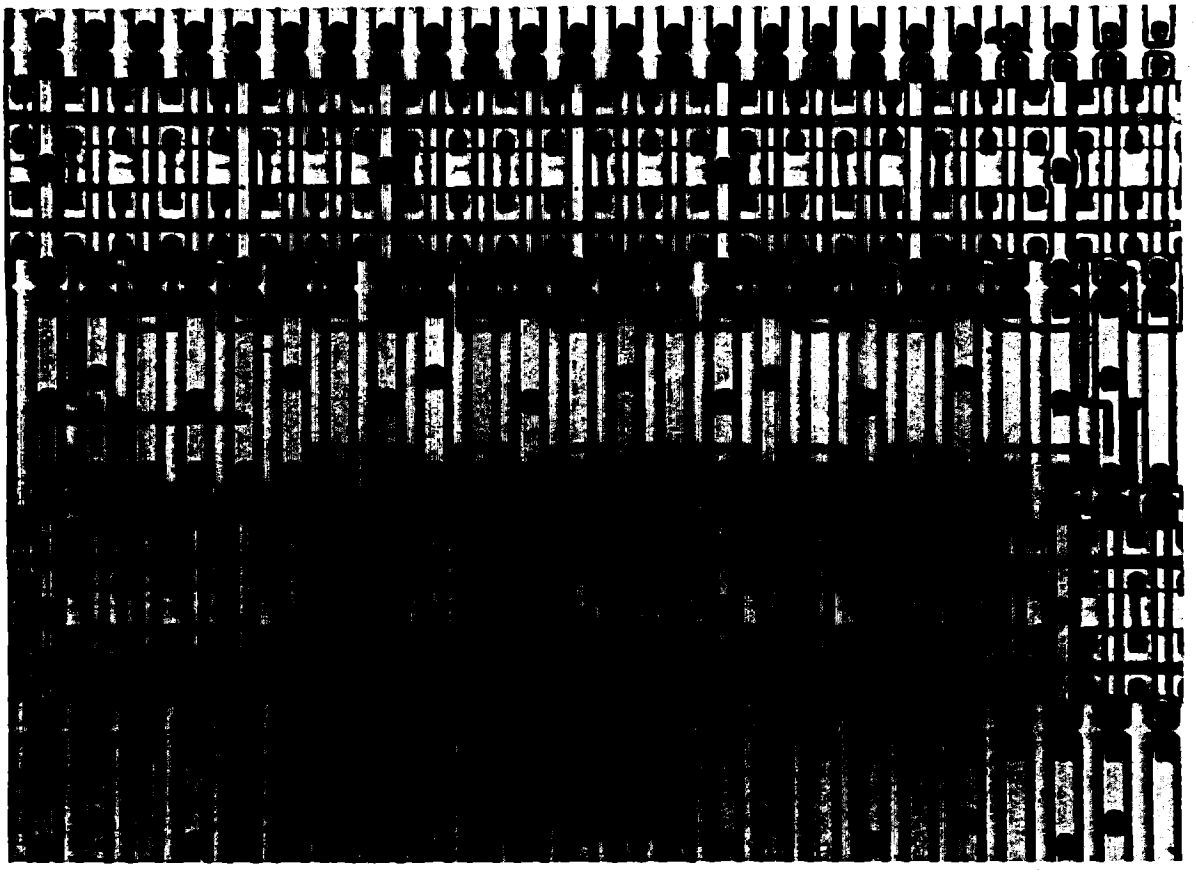

Figure 4. Light micrograph showing a single scan window portion of a 125-stage ring oscillator circuit. Device interconnects were fabricated by laser direct-write of n-doped polysilicon. Power, buses, via plugs, and output trace at left are photolithographed Al-Si alloy.

Interconnection of an entire gate array requires writing 50 to 100 scan windows of roughly 400-500 microns on a side. Each window required 4 - 5 seconds, including stage translation and settling. The time required to personalize a gate array is therefore a few hundred seconds. In particular, writing eight 125-stage ring oscillators was achieved in just under 5 minutes. Circuits with traces running between scan windows were demonstrated. Reliable connection of traces running between windows was achieved by superimposing traces at scan window boundaries.

Circuits with more complex interconnect structures, consisting of shift registers and counters, have been fabricated. In particular, several chips were fabricated having five 16-stage shift registers and one 16-stage counter on them. A light micrograph of one of these circuits fabricated with laser-deposited polysilicon is shown in Fig. 5. The basic building block of these circuits were D flip-flops and transmission gates. The counter and one of the shift registers were wired to output buffer ports at each stage to monitor sequential operation by electrical probing after interconnection. Electrical testing verified that these circuits functioned properly at a clock frequency of 1 MHz.

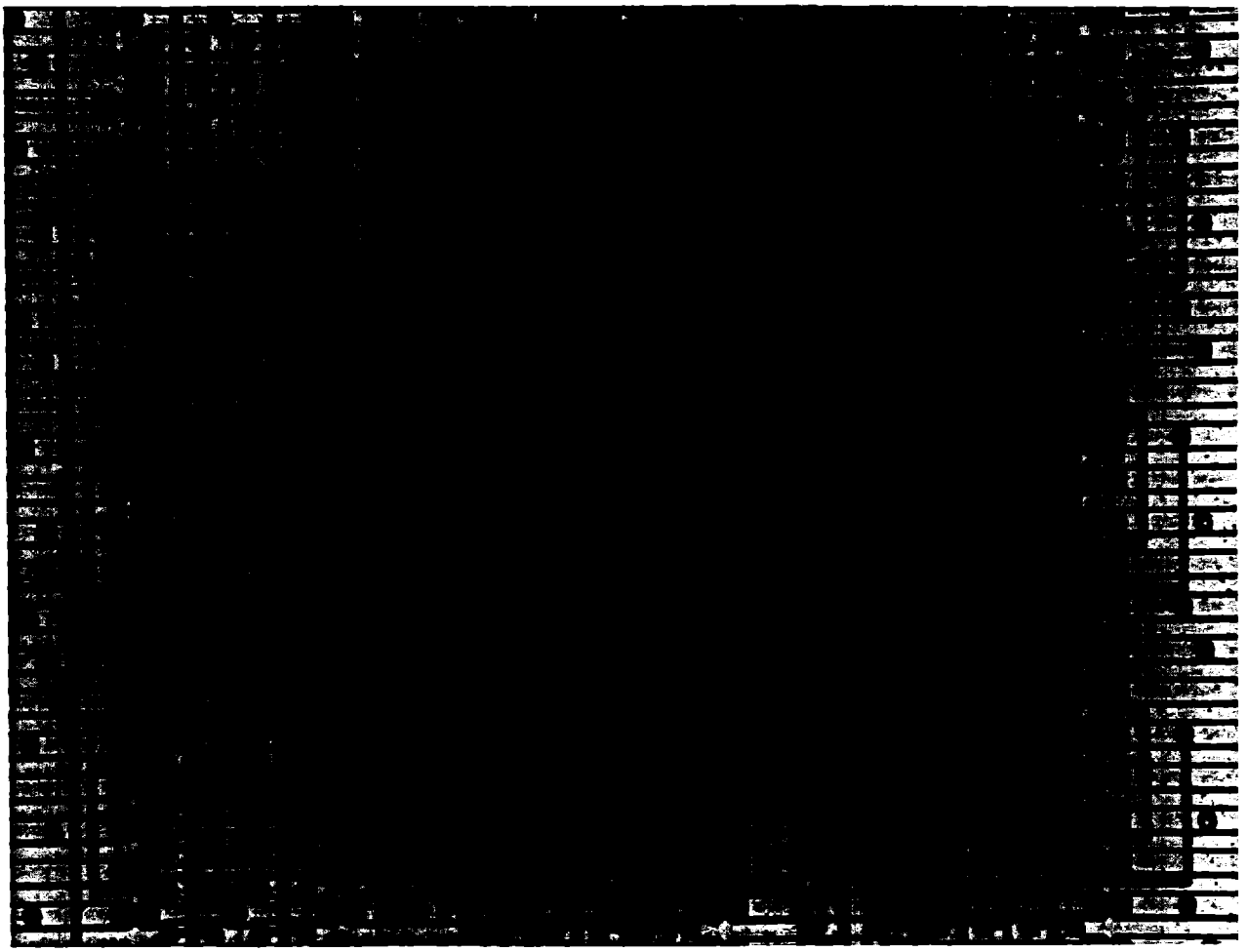

Figure 5. Light micrograph of part of shift register circuit described in text. Portions of two scan windows are shown.

VI. DISCUSSION

Typical digital circuits often require high density interconnect structures, in contrast to circuits used in our evaluation of the process properties. In particular, the 5 minute-per-die figure cited is minimal for the poly process. Maximum possible density interconnection of these 4 mm square die with a pitch of 11 μm would take (4000 μm)^2/(11 μm)(1000 μm/s) = 1455 s or ~24 minutes for line writing, with the worst-case addition of up to ~2 minutes for stage translation and settling. A more realistic time estimate for single level personalization of a complex circuit on gate arrays of these dimensions is 10-15 minutes.

All viable laser pyrolytic deposition processes for use in fabrication of IC interconnect structures need some means of accounting for the dramatic differences in thermal conductivity and optical absorption normally found between device contact, routing channel, and tunnel contact areas. Deposition of a thin film of a-Si as an absorbing layer greatly reduced the effects which underlying structures had on process parameters.

Since aluminum-silicon has very high thermal conductivity compared with a-Si, the a-Si served the dual function of heat retention (over vias and power buses), in addition to absorbing the incident laser power. The reaction still ran cooler over aluminum-silicon regions than over oxide regions, because a-Si does not completely shield the effect of the high thermal conductivity of the aluminum-silicon. The net result is that slightly less material will be deposited over aluminum-silicon regions, for a given dwell time, compared with oxide regions. Although we had the ability to alter process conditions over various structures, highly reliable laser direct-write interconnection of circuits was achieved using a single value for incident laser power everywhere.

The use of degenerately doped poly is limited to short interconnects, due to its low electrical conductivity. This process flow can be modified to achieve higher conductivity material by removing the a-Si in bulk after laser direct-write personalization. Selective tungsten CVD [18] may then be used to grow tungsten only where poly lines have been deposited. In particular, a thick selective tungsten CVD process [19] could yield conductivities sufficient for interconnecting high performance VLSI MOS circuits.

ACKNOWLEDGMENTS

Dave Ashkenas, Steve Farmwald, Rod Hyde, Irving Herman, Jim Kaschmitter, Harlan Lau, Jerrold Rittmann, and David B. Tuckerman made major contributions in helping to understand the engineering processes and equipment used in work reported. Contributions made by Bonnie K. Carnahan, Frederick D. Cook, Donald E. Duerre, Irving P. Herman, Richard Mendonca, A. Elon Ormsby, Wayne E. Tindall, and Jimmy C. Trevino are greatly appreciated. Also, thanks to Deborah Ross for expert assistance in preparing the manuscript.

Lowell L. Wood and A. Carl Haussmann have been instrumental in making this effort possible. The work was sponsored by DoE (through LLNL's IR&D Program) and DoD (through the VHSIC Program Office under Contract No. FY1175-85-N-5695, monitored by J. P. Letellier). John C. Whitehead was supported by the Fannie and John Hertz Foundation. Fred Mitlitsky was aided by Prof. Richard M. Osgood, Jr. and the Columbia University Electrical Engineering Department.

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